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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,301	05/31/2000	Frank P. Helms	1001-0119	3171

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EXAMINER
HO, THANG H

ART UNIT	PAPER NUMBER
2188	3

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/584,301	HELMS, FRANK P.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 January 2001 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Claims 1-34 are presented for examination.

2. The information disclosure statement (IDS) filed on 01/22/2001 have been received and considered. Please see attached PTO-1449.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "218" in figure 2 has been used to designate both "AGP CARD" and "HLDSREF#". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 13 and 17 are objected to because of the following informalities:

As per claim 13, on lines 2-3, the recitation of "at at least a first logical level" and "at a high impedance level" should be changed to read --to the first logical level-- and --to the high impedance level--, respectively.

As per claim 17, on lines 2-3, the recitation of "signal during to the isolation circuit the power savings state" should be changed to read --signal to the isolation circuit during the power savings state--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-13 and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Baweja et al. (USPN: 6,212,599), hereinafter Baweja.

As per claims 1 and 26, Baweja discloses in figure 2 the method for controlling a self-refresh state of memory in a computer system, comprising: controlling at least one memory control signal (260) being supplied to the memory from a first integrated circuit (210) in the computer system according to an operational state; and controlling the memory control signal from a second memory controller (220) in the computer system when the computer system is in a power savings state (e.g. column 4, lines 34-36), to maintain memory in the self-refresh state.

As per claim 2, Baweja discloses the method as in claim 1 wherein the first integrated circuit (figure 2, element 210) is completely powered off during the power savings state (e.g. column 3, lines 54-56, column 4, lines 34-37 and column 59-61).

As per claims 3 and 27, Baweja discloses the method as in claim 1 wherein the power savings state is a suspend to RAM state (e.g. column 4, lines 20-32).

As per claim 4, Baweja discloses the method as in claim 1 wherein the memory control signal is a clock enable signal (e.g. column 5, lines 6-15).

As per claim 5, Baweja discloses the method as recited in 1 wherein the memory control signal is reset signal (e.g. column 6, lines 22-et seq.).

As per claim 28, claim is rejected supra with respect to claims 4 and 5.

As per claim 6, Baweja discloses the method as recited in claim 4 wherein the clock enable signal is low while the memory is maintained in the self-refresh state (e.g. column 5, lines 9-13).

As per claims 7 and 29, Baweja discloses the method as recited in claim 1 wherein the memory control signal is held at a first value to keep the memory in the self-refresh state (e.g. column 5, lines 13-14).

As per claims 8 and 30, Baweja discloses in figure 2 the method as recited in claim 1 further comprising isolating the first integrated circuit from the memory during the power savings state wherein the isolating circuit is inherently embedded within the memory system controller (200) in order for the second memory controller (220) to control the memory control signal (260).

As per claim 9, Baweja discloses in figure 2 the method as recited in claim 8 wherein isolating further includes disabling a switch, wherein the switch capable of outputting high-impedance level is inherent in order to isolate the clock enable signals between the two memory controllers (210 and 220), coupling the memory control signal (260) from the first integrated circuit (210) to the memory (225) by driving a switch enable signal to a first predetermined value to turn off the switch, the switch enable signal being driven from the second memory controller (e.g. see also column 5, lines 16-22).

As per claim 10, Baweja discloses in figure 2 the method as in claim 9 further comprising driving a signal line which is coupled to the switch and is coupled to the memory control signal input (260) to the memory (element 225) to a predetermined logical level from the second memory controller (220), during the power savings state to control the memory control signal and wherein the signal line is driven at a high-impedance by the second memory controller (220) during the operational state (e.g. column 5, lines 16-22).

As per claim 11, Baweja discloses the method as in claim 10 wherein the switch enable signal is at a second predetermined value to turn on the switch during the operational state (e.g. column 5, lines 16-22).

As per claim 12, Baweja discloses in figure 2 the method as in claim 9 wherein the second memory controller (220) drives the signal line coupled to the switch and coupled to the memory control signal input (260) to the memory (225) before the switch enable signal is driven to the first predetermined value to turn off the switch and wherein the switch enable signal is driven to the second predetermined value to turn on the switch

before the second memory controller drives the signal at high impedance (e.g. column 5, lines 16-22).

As per claim 13, Baweja discloses in figure 2 the method as in claim 1 wherein the first integrated circuit (210) drives the memory control signal (260) at least a first logical level during the operational state and the second memory controller (220) drives the memory control signal (260) at a high impedance level during the operational state and wherein the first integrated circuit (210) is powered off during the power savings state and the second memory controller drives the memory control signal (260) at a second logical level during the power savings state, to keep the memory in the self-refresh state (e.g. column 3, lines 54-56, column 4, lines 34-37,column 59-61 and column 5, lines 16-22).

As per claims 14-22, 31 and 34, the claims encompass the same scope of invention as to that of claims 1-13, however the claims are drafted as apparatus format rather than method format, the claims are therefore rejected for the same reasons as being set forth above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al. (USPN: 6,212,599), hereinafter Baweja.

As per claims 32 and 33, Baweja discloses the system and method above. However, Baweja does not specifically disclose the application of integrated circuit (IC) to dispose the memory control circuit, the second circuit and the CPU on one IC. Nevertheless, it is well known in the art that IC technologies allow designers to fit multiple components including the memory control circuit, the second circuit and the CPU onto a single chip to prevent cross-signaling and to reduce access latency thereby improving the overall system performance. It would have been prima facie obvious for one skilled in the art at the time the invention was made to dispose the memory control circuit, the second circuit and the CPU on a single IC into the system and method by Baweja to generate the claimed invention with a reasonable expectation of success for the purpose stated above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

After-final	(703) 746-7238
Official	(703) 746-7239
Non-Official/Draft	(703) 746-7240

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-6606 for regular communications and 703-308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

TH
July 21, 2003

Kevin L. Ellis
Primary Examiner

Kevin L. Ellis